

GR-10Z011FQ: 100V High-low Side GaN with Integrated Driver

Description

The GR-10Z011FQ is a Gallium Nitride (GaN) FET with integrated driver. The device features High-side and low-side 100V rated GaN FET driven by an optimized high-frequency GaN FET driver. The GR-10Z011FQ incorporates an high-side level shifter and bootstrap circuit. This integration allows GR-10Z011FQ unit to form a half-bridge topology without the need for external level-shifting circuit. The driver and the GaN FET are mounted using Flip-chip bond packaging technology, resulting in minimized package parasitic elements.

Key Specifications

Part Number	GR-10Z011FQ
V _{DSS} , min.	100V
R _{DS(ON)} , typ.	11mΩ (HS & LS FET)
Package	QFN-3.5 x 5.0

Features

- Gate drive voltage compatibility
- High operating frequency
- Over temperature protection
- Short circuit protection
- 20 ns typical delay time

Applications

- Buck, boost, buck-boost converters
- AC-DC/ DC-DC Converters
- Motor Drives

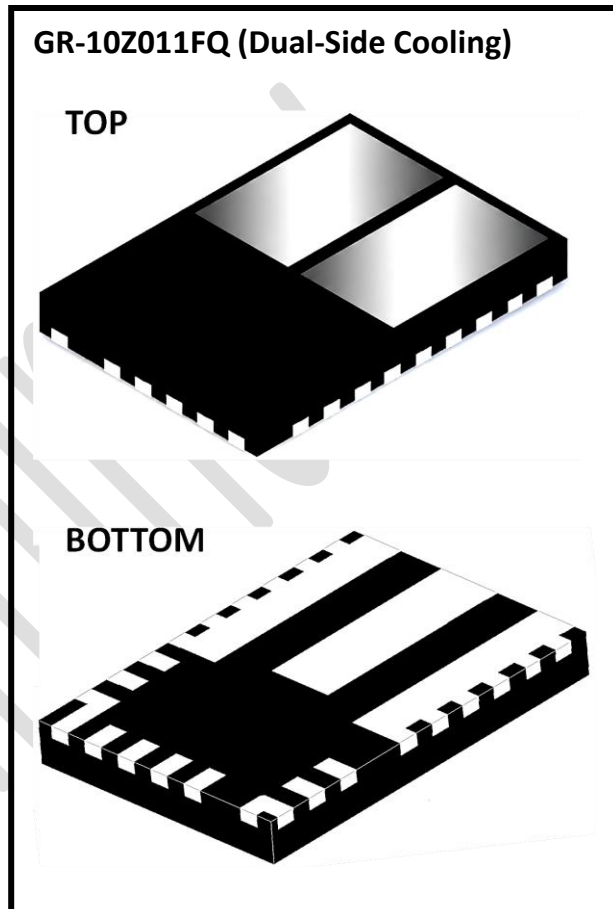
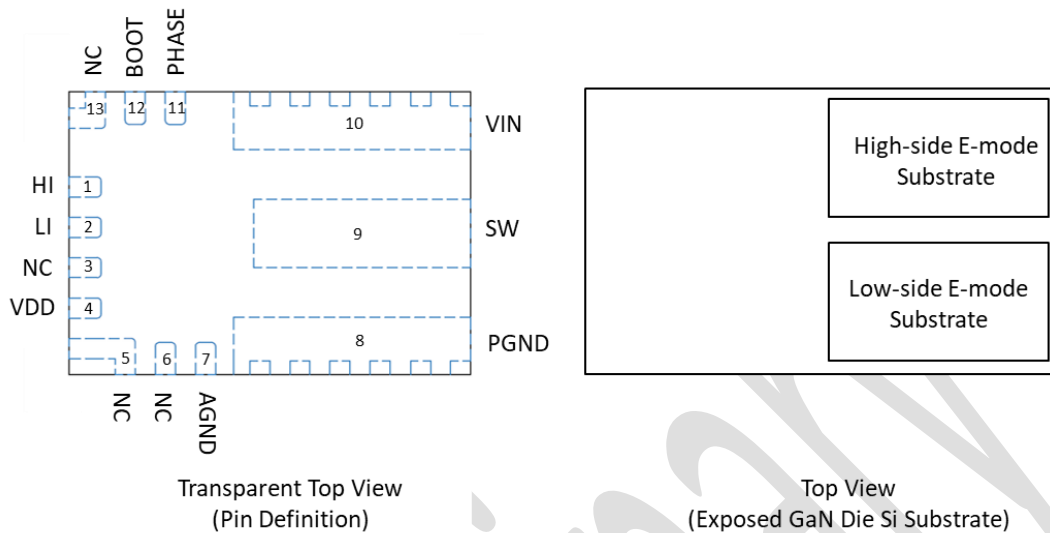


Table of Contents

	Description	1
	Key Specifications	1
	Features.	1
	Applications	1
	Table of Contents	2
1	Pinout Configuration and Description	3
2	Absolute Maximum Rating	4
3	Specification	5
4	Package Outline Dimensions	8
5	Change Log.	9

1- Pinout Configuration and Description



Pin Name	Pin	I/O/P	Description
HI	1	I	High Side Driver PWM Input. Connect this pin to the high side driver control PWM input.
LI	2	I	Low Side Driver PWM Input. Connect this pin to the low side driver control PWM input.
NC	3,5,6,13	-	No connection. Do not connect to any circuit. It is recommended that these pins be left floating.
VDD	4	P	Supply Voltage for the IC. This pin provides bias voltage for the IC. Connect this pin to 5V voltage source with at least 1uF MLCC bypass capacitor.
AGND	7	G	Ground for the IC. All voltage levels are measured with respect to this pin.
PGND	8	G	Input power supply ground return. Connected to source terminal of internal low side FET. Connect power loop capacitors from VIN to PGND.
SW	9	P	Output switching node. Connected to output of half-bridge power stage. SW pin connects the source terminal of high side FET and the drain terminal of the low side FET.
VIN	10	P	VIN Power input. Connected to drain terminal of internal high side FET. Connect power loop capacitors from VIN to PGND or power source terminals of low side FET.
PHASE	11	P	PHASE Switch Node. Connect this pin to the source of the upper GaN FET and the drain of the lower GaN FET. This pin is used as the return path for the UGATE driver.
BOOT	12	P	Bootstrap Supply. For the floating upper gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper GaN FET. Make sure that C_{BOOT} is placed near the IC.

2- Absolute Maximum Rating

Specification	MIN	MAX	Unit
VIN to SW		100	V
VIN to SW (5ms pulses at 150°C)		120	V
BOOT to AGND	-0.3	V _{PHASE} + V _{CC}	V
SW to PGND (DC)	-0.3	100	V
SW to PGND (<25ns)	-5	105	V
HI to AGND	-0.3	6.6	V
LI to AGND	-0.3	6.6	V
VDD to AGND	-0.3	6.6	V
BOOT to PHASE	-0.3	6.6	V
BOOT to PHASE (<25ns)	-0.3	7.0	V
Junction Temperature, T _J	-40	150	°C
Storage Temperature, T _S	-40	150	°C

3- Specification

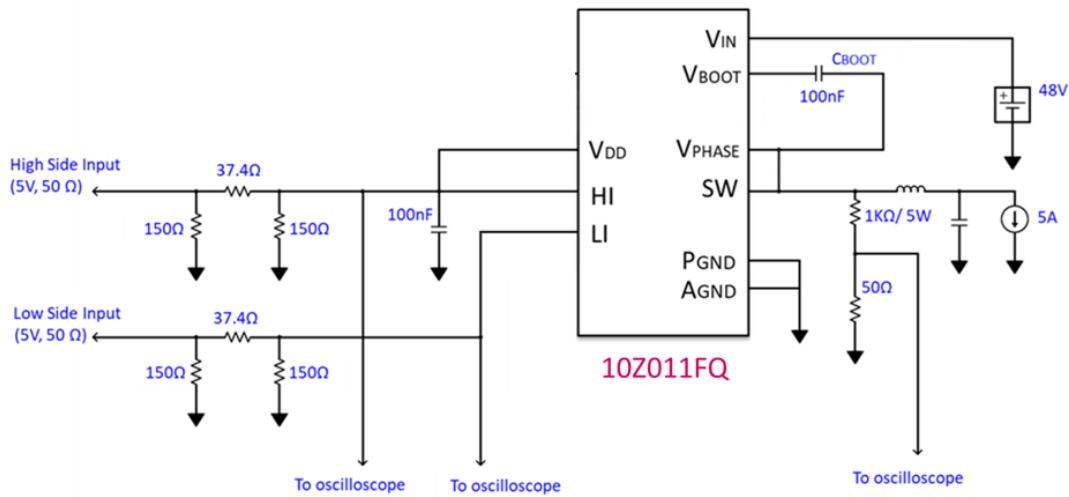
3.1 Electrical Characteristics

(VDD=VBOOT=5V, VGND=VPHASE=0V, T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Values			Unit
			Min	Typ	Max	
High Side Internal Power FET						
RDS(on)_HS	High Side FET RDS(on)	I _{LOAD} = +/-10A, HS _{IN} = 5V, LS _{IN} = 0V	-	8.6	11	mΩ
VHS_DS_Clamp	High Side 3rd Quadrant Clamp	I _{LOAD} = - 10A, HS _{IN} & LS _{IN} = 0 V	-	-1.5	-	V
ILEAK_VIN-SW	Leakage Current (VIN to SW)	HS _{IN} = 0V, V _{IN} = 100V, SW = 0 V	-		300	μA
CWELL	HV-Well Capacitance (SW to PGND)	HS _{IN} = 0V, V _{IN} = 48V, SW = 48 V	-	33	-	pF
COSS_HSFET	Output Capacitance (VIN to SW)	HS _{IN} = 0V, V _{IN} = 48V, SW = 0 V	-	192	-	pF
QOSS_HSFET	Output Charge (VIN to SW)	HS _{IN} = 0V, V _{IN} = 48V, SW = 0 V	-	15	-	nC
Low Side Internal Power FET						
RDS(on)_LS	Low Side FET RDS(on)	I _{LOAD} = +/-10A, LS _{IN} = 5V, HS _{IN} = 0V		8.6	11	mΩ
VLS_DS_Clamp	Low Side 3rd Quadrant Clamp	I _{LOAD} = - 10 A, HS _{IN} & LS _{IN} = 0 V		-1.5		V
ILEAK_SW-PGND	Leakage Current (SW to PGND)	LS _{IN} = 0V, V _{IN} = 100V, SW = 100 V			100	μA
COSS_LSFET	Output Capacitance (SW to PGND)	LS _{IN} = 0 V, SW = 48 V		192		pF
QOSS_LSFET	Output Charge (SW to PGND)	LS _{IN} = 0 V, SW = 48 V		15		nC
Dynamic Characteristics						
t _{delayHS_on}	High-Side On Propagation Delay	SW = 0 V and HS FET Turn-On, R _{BOOT} = 2.2Ω, I _{LOAD} = 5A		20		ns
t _{delayLS_on}	Low-Side On Propagation Delay	SW = 48 V and LS FET Turn-On, I _{LOAD} = 5A		20		ns
t _{delayHS_off}	High-Side Off Propagation Delay	SW = 48 V and HS FET Turn-Off, I _{LOAD} = 5A		20		ns
t _{delayLS_off}	Low-Side Off Propagation Delay	SW = 0 V and LS FET Turn-Off, I _{LOAD} = 5A		20		ns
t _{matchon}	Delay Matching LSoft to HSon	LS Turn-Off to HS Turn-On, R _{BOOT} = 2.2Ω, I _{LOAD} = 5A		0		ns
t _{matchoff}	Delay Matching HSoft to LSon	HS Turn-Off to LS Turn-On, I _{LOAD} = 5A		0		ns
t _{riseSW_HS0}	SW Rise Time at High Side FET Turn-On (Buck Mode, Hard Switching)	HS Turn-On Buck Mode, 0V to 48V, R _{BOOT} = 0Ω, I _{LOAD} = 5A		1.5		ns
t _{riseSW_HS1}		HS Turn-On Buck Mode, 0V to 48V, R _{BOOT} = 2.2Ω, I _{LOAD} = 5A		3		ns
t _{fallSW_LS0}	SW Fall Time at Low Side FET Turn-On (Boost Mode, Hard Switching)	LS Turn-On Boost Mode, 48V to 0V, I _{LOAD} = 5A		1.5		ns
t _{fallSW_LS1}		LS Turn-On Boost Mode, 48V to 0V, I _{LOAD} = 5A		3		ns
Bootstrap Power Supply						
I _{BOOT_Q}	Off State Bootstrap Supply Current	HS _{IN} /LS _{IN} = 0V, (V _{BOOT} - V _{PHASE}) = 5V	-	0.1	0.12	mA
I _{BOOT}	Bootstrap Supply Current @100k	HS PWM = 500 kHz, C _{LOAD} = 0nF	-	1.5	2.5	mA
I _{QBOOTG}	BOOT to PHASE Leakage Current	HI=LI=0V, VPHASE=VBOOT=100V		0.3		uA

Symbol	Parameter	Conditions	Values			Unit
			Min	Typ	Max	
Power On Reset						
VDD_POR+	POR Trip Level VDD Rising	LS _{IN} = 5V, V _{DD} Ramps Up	3.8	4	4.2	V
VDD_POR_HYST	POR V _{DD} Falling Hysteresis	LS _{IN} = 5V, V _{DD} Ramps Down	-	0.3	-	V
VBOOT_POR+	POR Trip Level (V _{BOOT} - V _{PHASE}) Rising	HS _{IN} = 5V, V _{BOOT} Ramps Up	2.5	3.4	3.9	V
VBOOT_POR_HYST	POR (V _{BOOT} - V _{PHASE}) Falling Hysteresis	HS _{IN} = 5V, V _{BOOT} Ramps Down	-	0.2	-	V
Logic Input Pins						
PW_min	Minimum Input On or Off Pulse Duration	50% to 50% width, L _{IN} and H _{IN}	30	-	-	ns
PW_max	Maximum Input On or Off Pulse Duration	50% to 50% width, L _{IN} and H _{IN}	-	-	200	µs
VIH	High-level Logic Threshold	HS _{IN} , LS _{IN} Rising	2.4	-	-	V
VIL	Low-level Logic Threshold	HS _{IN} , LS _{IN} Falling	-	-	0.8	V
VIHYST	Logic Threshold Hysteresis	V _{IH} Rising - V _{IL} Falling	-	0.2	-	V

Dynamic Characteristics Parameter Definition



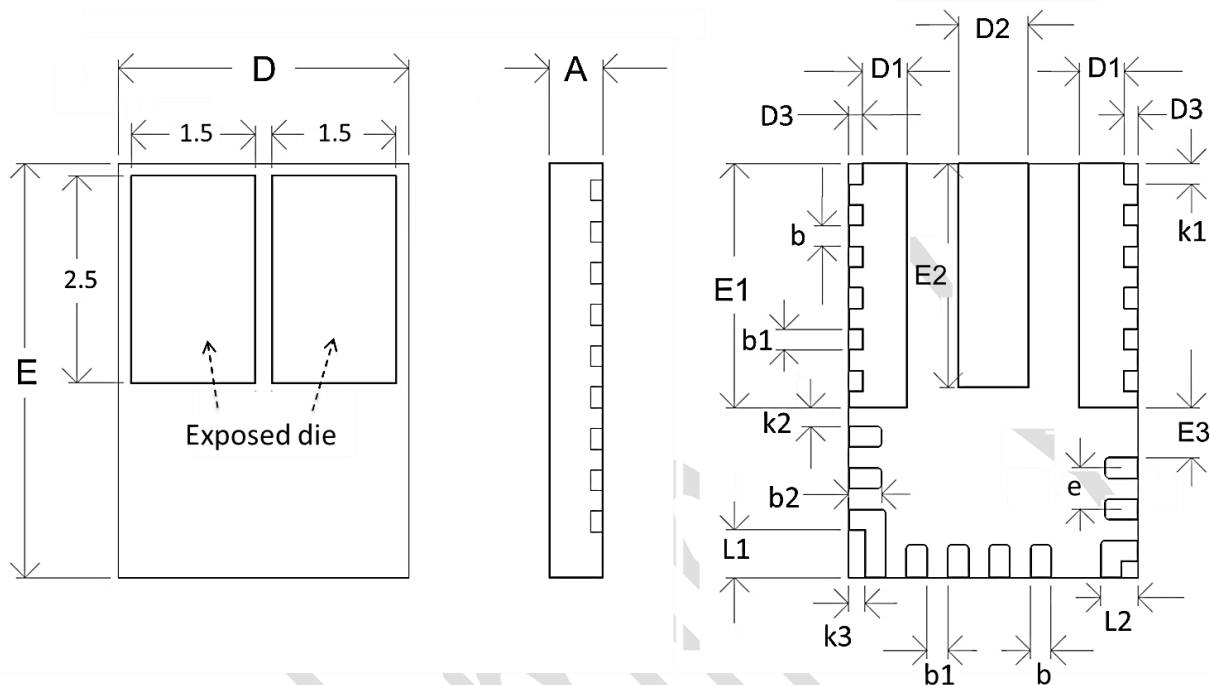
3.2 Thermal Information

Symbol	Parameter	Value	Unit
R _{θJA}	Junction-to-ambient thermal resistance	38.5	°C/W
R _{θJC}	Junction-to-case (top) thermal resistance	0.45	°C/W
R _{θJB}	Junction-to-board thermal resistance	16	°C/W
R _{θJC(Bot)}	Junction-to-case (Bottom) thermal resistance	3.3	°C/W

3.3 ESD Ratings

Symbol	Parameter	Value	Unit
HBM	Human Body Model	1000	V
CDM	Charged Device Model	500	V

4- Package Outline Dimensions



Dimension of GR – 10Z011FQ

SYMBOL	DIMENSION (MM)			SYMBOL	DIMENSION (IN MM)		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	--	0.65	0.70	E1	2.85	2.95	3.05
b	0.15	0.25	0.35	E2	2.60	2.70	2.80
b1	0.15	0.25	0.35	E3	0.50	0.60	0.70
b2	0.30	0.40	0.50	e	0.50 BSC		
D	3.40	3.50	3.60	K1	0.150	0.250	0.350
E	4.90	5.00	5.10	K2	0.125	0.225	0.325
L1	0.475	0.575	0.675	K3	0.100	0.200	0.300
L2	0.35	0.45	0.55				
D1	0.44	0.54	0.64				
D2	0.74	0.84	0.94				
D3	0.07	0.17	0.27				

5- Change Log

Version	Date	Description
01	Dec 1, 2025	Initial version

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